

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Eigo NAKAGAWA et al.

Application No.: New U.S. Patent Application

Filed: November 26, 2003

Docket No.: 117863

For: CIRCUIT BOARD INSPECTION DEVICE

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Pursuant to 37 CFR §1.56, the attention of the Patent and Trademark Office is hereby directed to the reference(s) listed on the attached PTO-1449. Unless otherwise indicated herein, one copy of each reference is attached. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the reference(s) be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

- 1. This Information Disclosure Statement is being filed (a) within three months of the U.S. filing date of this non-CPA application, OR (b) before the mailing date of a first Office Action on the merits in the present application. No certification or fee is required.
- 2. Relevance of the non-English language references are discussed in the present specification. (Refs. 1-3)
- 3. English-language Abstracts of the non-English language references are attached hereto. (Refs. 1-2)
- 4. Computer-generated English translations of the following Japanese Patent Publications have been obtained from the website of the Japanese Patent Office (<http://www.jpo.go.jp>), and are attached, but have not been reviewed for accuracy. See References 1-2.

Respectfully submitted,

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Date: November 26, 2003

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Form PTO-1449 (REV. 8-83)		US Dept. of Commerce PATENT & TRADEMARK OFFICE	ATTY DOCKET NO. 117863	APPLICATION NO. New U.S. Patent Application		
INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)						
		APPLICANTS Eigo NAKAGAWA et al.				
		FILING DATE November 26, 2003				
U.S. PATENT DOCUMENTS						
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS
FOREIGN PATENT DOCUMENTS						
		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS
	1	JP A 2000-74998 w/ abst & trans	03/14/2000	Japan		
	2	JP A 11-038111 w/ abst & trans	02/12/1999	Japan		
OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)						
	3	"Detection of Flaws in a Printed Circuit Board by Using an Eddy-Current Testing Approach" H. Fujiki et al; http://www.magmac1.ec.t.kanazawa-u.ac.jp/magcap-j/research-j/ecta-j.html				
EXAMINER					DATE CONSIDERED	
Examiner: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.						